



SHAPING THE NEXT GENERATION OF ELECTRONICS

**JUNE 23-27, 2024**

MOSCONE WEST CENTER  
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# Shift Left with Improved Power-Awareness in RTL Stage Design for Early Design Verification

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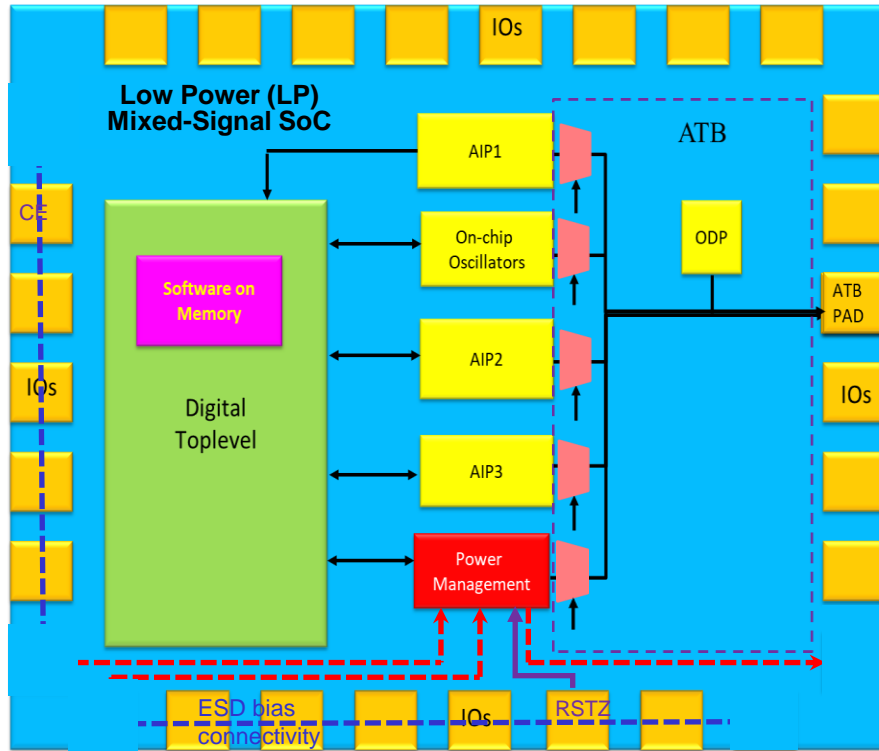
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Texas Instruments (India) Pvt. Ltd.

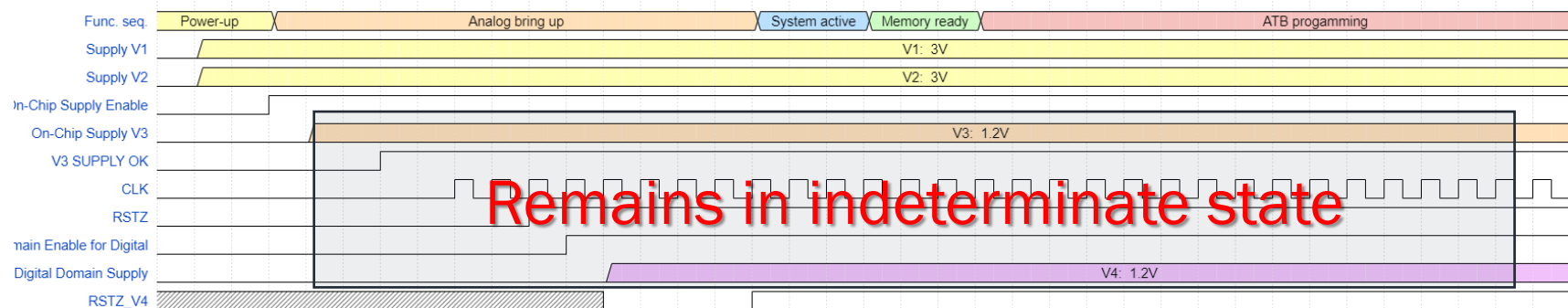




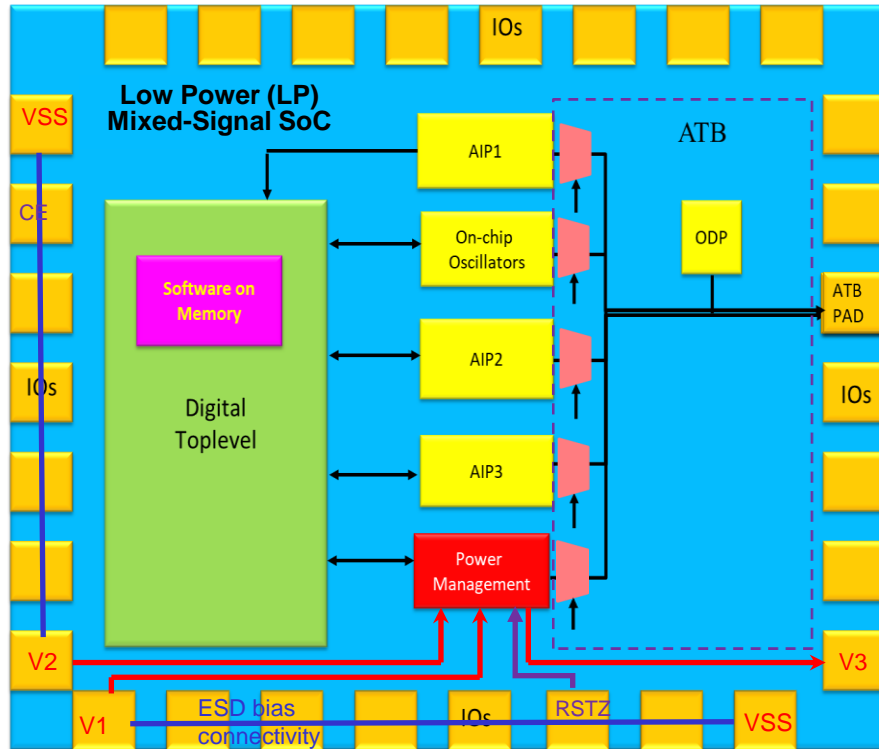
# Problem Statement & Motivation (1/2)



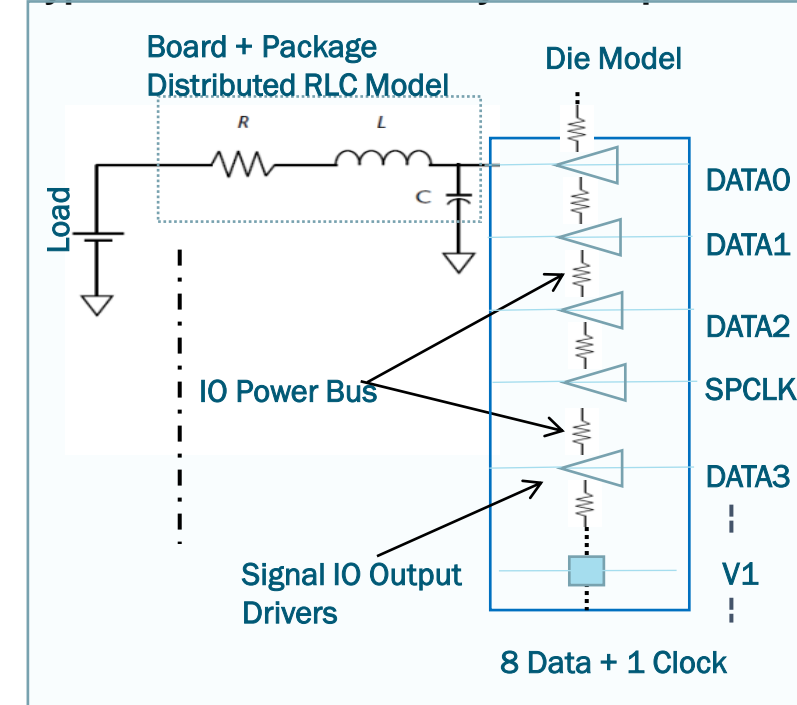
- Power and ground IOs' (PGIO)
  - ESD bias, trigger signal from PGIO → Drives IO protection devices
  - ESD bias affects chip enable (CE), reset (RSTZ) and external signal propagation
  - Multiple or split input/output (IO) pin supply rail requirements add to the complexity
  - Conventionally introduced as physical cells post synthesis and not part of RTL
- Conventional power aware (PA) RTL DMS & AMS co-sim.
  - ESD bias & Split IO rail functionality cannot be verified → Voltage level, transition times and sequencing
  - Initial power-up **fails without test-bench force** → Missing CE/RSTZ propagation
- PA Gate-Level (GL) simulation needed for complete verification



# Problem Statement & Motivation (2/2)



Typical Custom SSO Analysis Setup for SoC



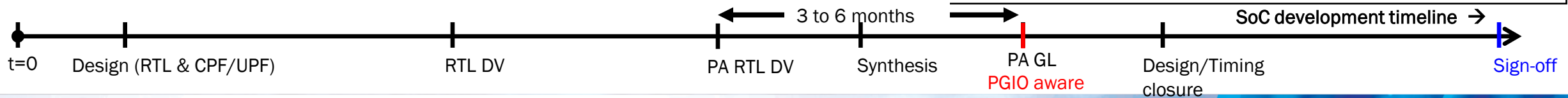
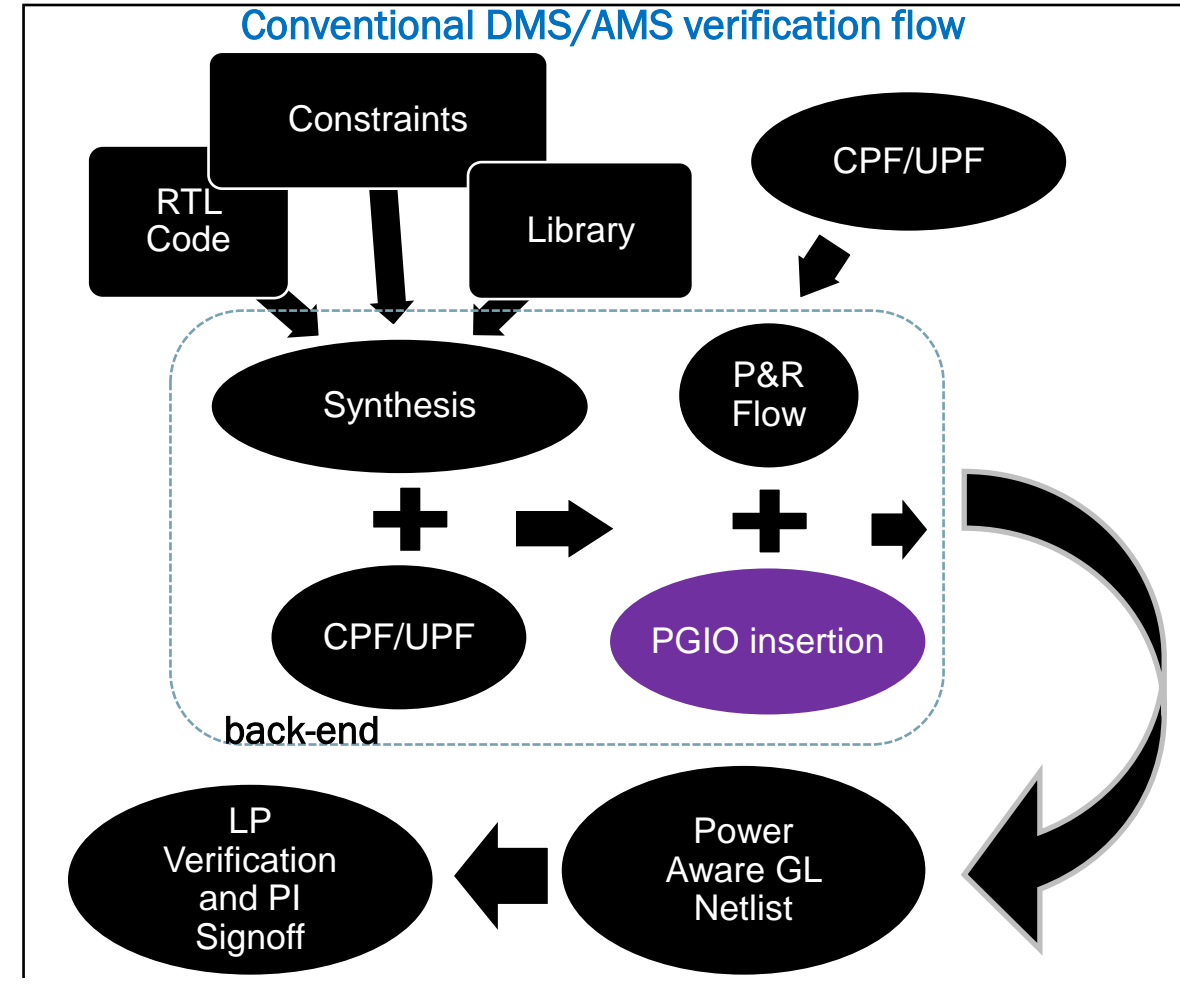
- Simultaneous switching output (SSO) of signal IOs cause signal and power integrity issues → Overshoots/undershoots,  $V_{IH}/V_{IL}$ , ground bounce etc.
  - Important with high speed IOs, common in Digital/Mixed-signal SoCs
  - Supply slew rate & overshoots/undershoots → ESD evaluation at early stage not possible
  - Analysis done **after implementation**, with **custom setup** → May not track actual design, and cause late changes

# Conventional DMS/AMS Verification - Limitations

- Conventional early simulations are based on RTL stage integration → Digital RTL & Power Intent (PI) as CPF/UPF
- Require custom test-bench forces for PGIO dependent signals  
E.g. ESD bias - ESD protection trigger for signal IO
- No direct equivalence to design as this aspect will itself evolves at later stage
- Complete verification possible only at GL stage hence “late verification closure”
- Informal link between assumptions in RTL verification vs actual implementation

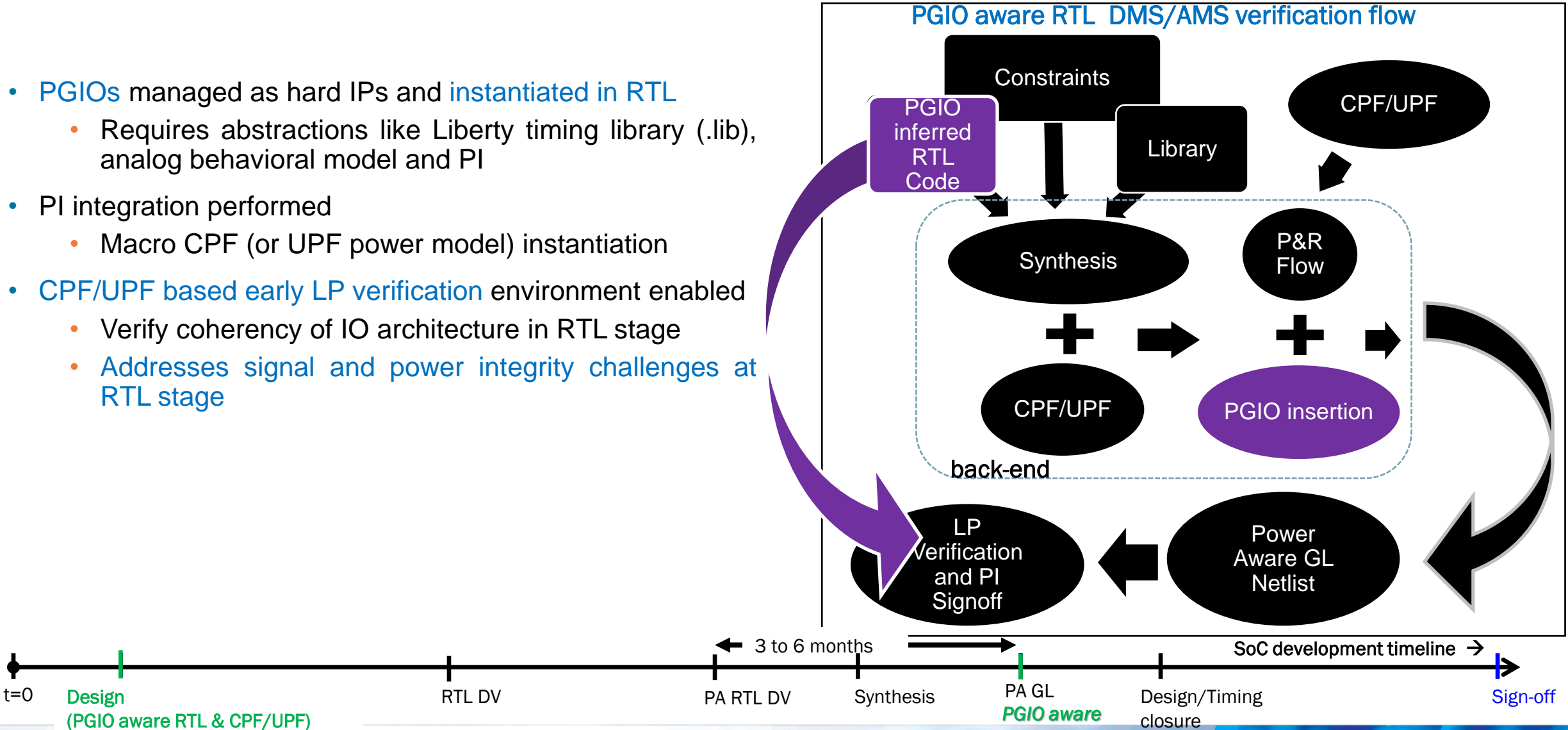
## References:

1. Lakshmanan B et al., “Extended Power Connectivity Solution for CPF based Low Power Simulation,” DAC 2021
2. Sooraj Sekhar et al., “Optimal and Efficient Power Aware Verification Framework for Low Power Mixed-Signal SoC,” DAC 2022



# Proposed PGIO aware RTL DMS/AMS verification

- PGIOs managed as hard IPs and **instantiated in RTL**
  - Requires abstractions like Liberty timing library (.lib), analog behavioral model and PI
- PI integration performed
  - Macro CPF (or UPF power model) instantiation
- **CPF/UPF based early LP verification** environment enabled
  - Verify coherency of IO architecture in RTL stage
  - **Addresses signal and power integrity challenges at RTL stage**



# Power Intent Capture: PGIO Domain Mapping

- All PGIOs (VDDS & VSS) are made part of PI at early RTL stage
- Power, ground connectivity at RTL stage - Enables ESD triggering simulations
- Enabled logical CLP checks at RTL stage
  - IO architecture completeness including PGIO
  - Split rail functionality
  - Mapping of different power supplies (E.g. ESD bias)
  - PI versus physical implementation coherency

```
set_macro_model VDDS33_PWR_80UM
#set_floating_ports { BIASFET_3P3V }
create_nominal_condition -name N1 -voltage 1.28 -ground_voltage 0
create_nominal_condition -name N2 -voltage 3.3 -ground_voltage 0
create_nominal_condition -name OFF -voltage 0 -ground_voltage 0 -state off
create_power_domain -name PAD_GP_BUS_VDD_1P2V_VSS
create_power_domain -name PAD_GP_VDDS_3P3V_VSS
create_power_domain -name PAD_GP_BIASFET_VSS -power_source \
    -shutoff_condition "BIASFET<1.318" -base_domains {PAD_GP_VDDS_3P3V_VSS}
update_power_domain -name PAD_GP_BUS_VDD_1P2V_VSS -primary_power_net BUS_VDD \
    -primary_ground_net VSS
update_power_domain -name PAD_GP_VDDS_3P3V_VSS -primary_power_net VDDS \
    -primary_ground_net VSS
update_power_domain -name PAD_GP_BIASFET_VSS -primary_power_net BIASFET \
    -primary_ground_net VSS
create_power_mode -name PM1 -default -domain_conditions { \
    PAD_GP_BUS_VDD_1P2V_VSS@N1 PAD_GP_VDDS_3P3V_VSS@N2 PAD_GP_BIASFET_VSS@N2 }
create_power_mode -name PM2 -domain_conditions { PAD_GP_BUS_VDD_1P2V_VSS@N1 \
    PAD_GP_VDDS_3P3V_VSS@OFF PAD_GP_BIASFET_VSS@OFF }
create_power_mode -name PM3 -domain_conditions { PAD_GP_BUS_VDD_1P2V_VSS@OFF \
    PAD_GP_VDDS_3P3V_VSS@N2 PAD_GP_BIASFET_VSS@N2 }
create_power_mode -name PM4 -domain_conditions { PAD_GP_BUS_VDD_1P2V_VSS@OFF \
    PAD_GP_VDDS_3P3V_VSS@OFF PAD_GP_BIASFET_VSS@OFF }
end_macro_model
```

UPF power models

UPF supply connections

UPF VCTs

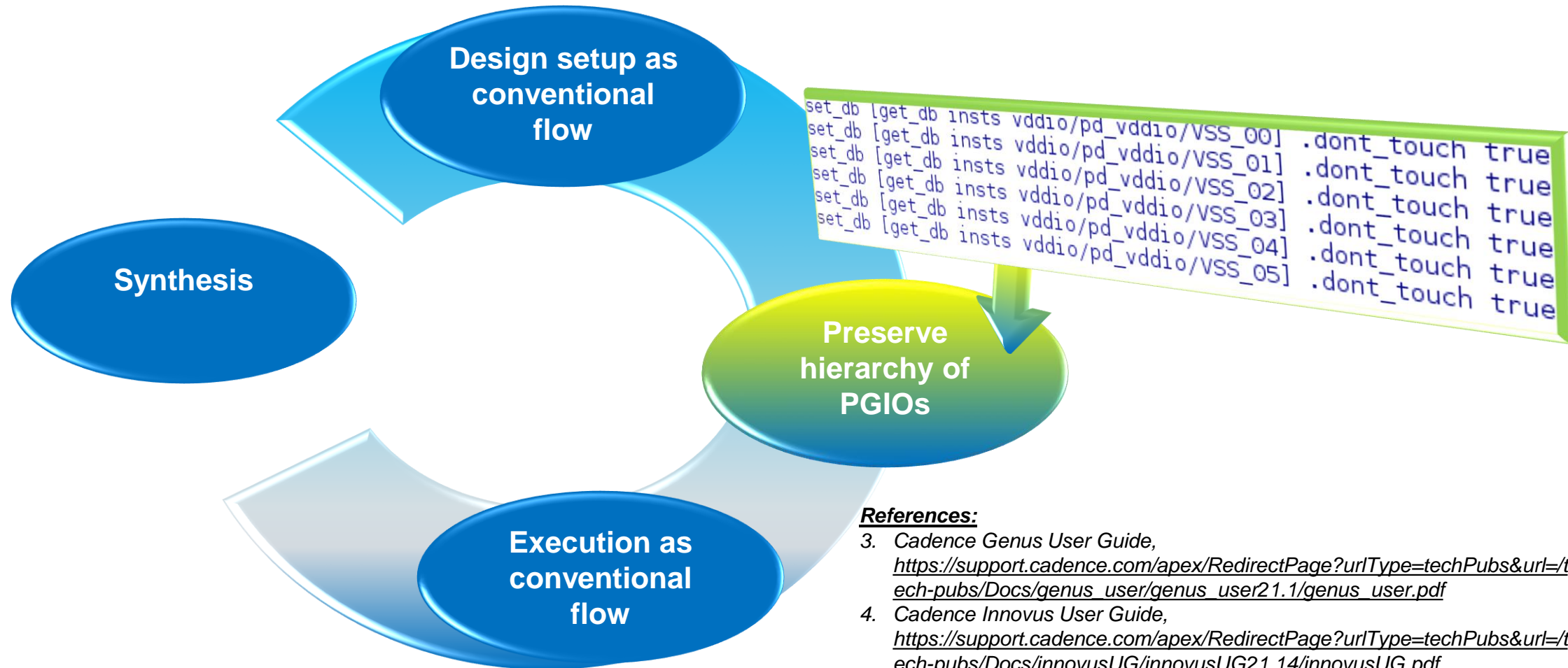
UPF power states

*\*Note: CPF macro model illustrated; Equivalent UPF artefacts identified*



# Handling PGIO in Synthesis

*Don't touch and preserve hierarchy of PGIO instances*



## References:

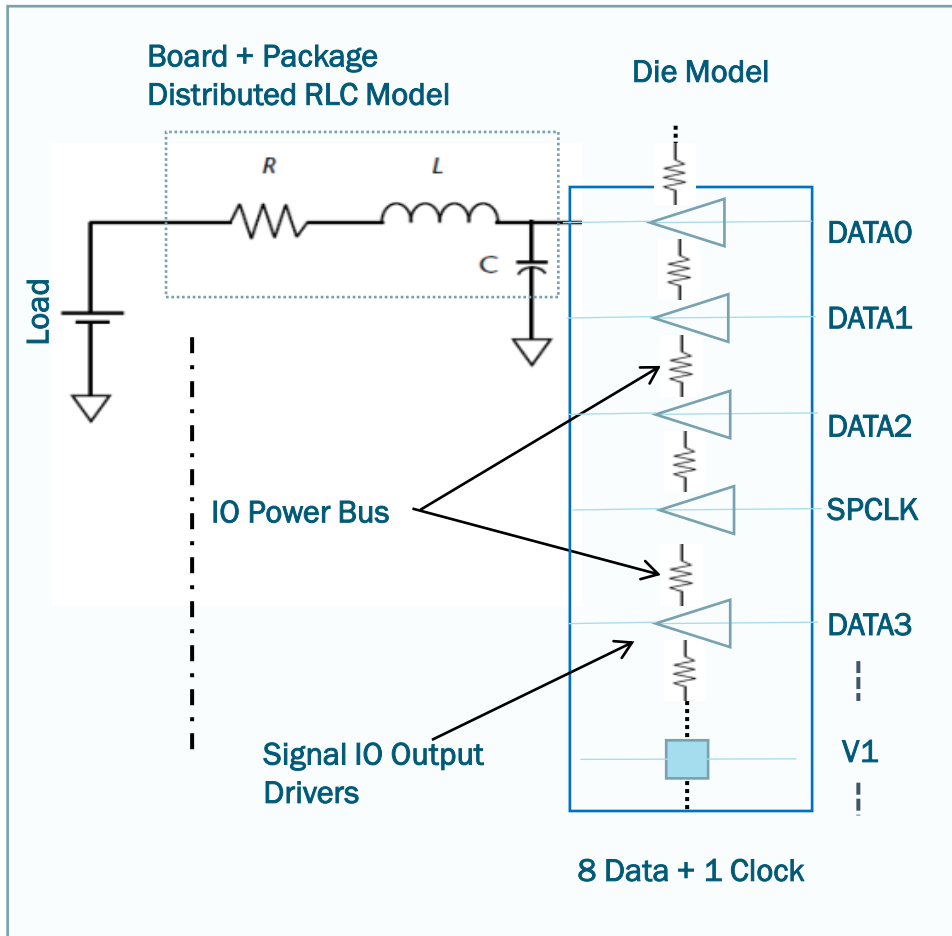
3. Cadence Genus User Guide,  
[https://support.cadence.com/apex/RedirectPage?urlType=techPubs&url=/tech-pubs/Docs/genus\\_user/genus\\_user21.1/genus\\_user.pdf](https://support.cadence.com/apex/RedirectPage?urlType=techPubs&url=/tech-pubs/Docs/genus_user/genus_user21.1/genus_user.pdf)
4. Cadence Innovus User Guide,  
<https://support.cadence.com/apex/RedirectPage?urlType=techPubs&url=/tech-pubs/Docs/innovusUG/innovusUG21.14/innovusUG.pdf>

*All physical design steps similar to conventional approach*



# Correct-by-Construct Early SSO Analysis

## Typical Custom SSO setup for SoC

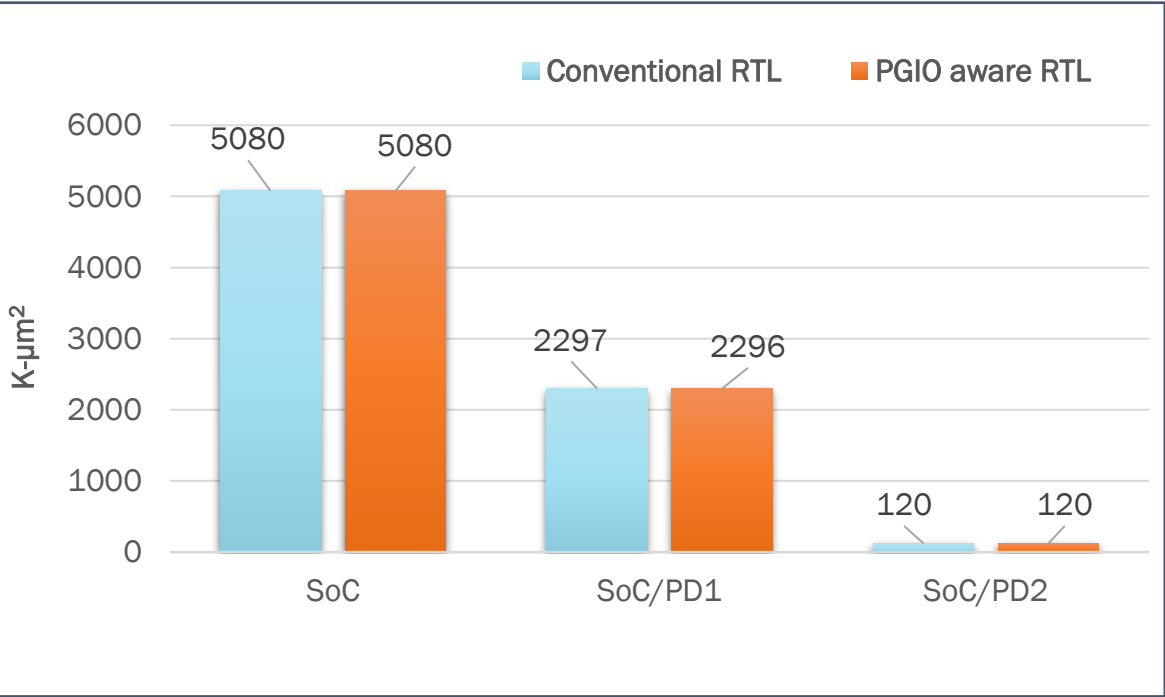


- PGIO instantiated RTL & power intent (CPF or UPF) → Enables early stage correct-by-construct SSO setup → Eliminates custom setup
  - Die, package & board aware simulations
  - Identifies the risks like signal IO and supply overshoots/undershoots and ground bounce due to simultaneous switching peak currents
- Early feedback to pinout changes for high speed interfaces (e.g. OSPI DDR) → Matures at RTL instead of post-synthesis stage
  - Additional supply/ground pins to meet signal and power integrity goals
  - Pin location change for sensitive signals
- Signoff analysis tracks actual design maturity
  - Handle early at RTL stage & avoid custom analysis

# Evidence: Results

- PGIO aware SoC RTL has been taken through entire physical design (PD) cycle
- Minor placement changes between two runs → negligible variation in the timing
- ***No impact to area, timing and conventional flow execution***

Area



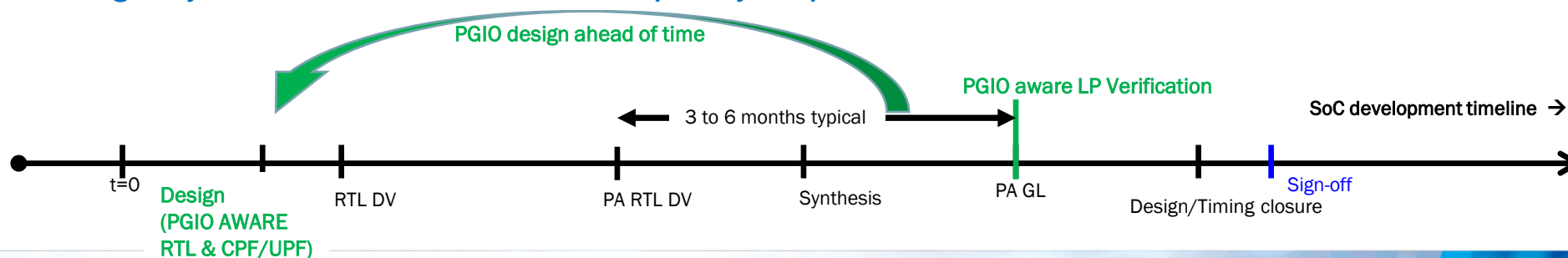
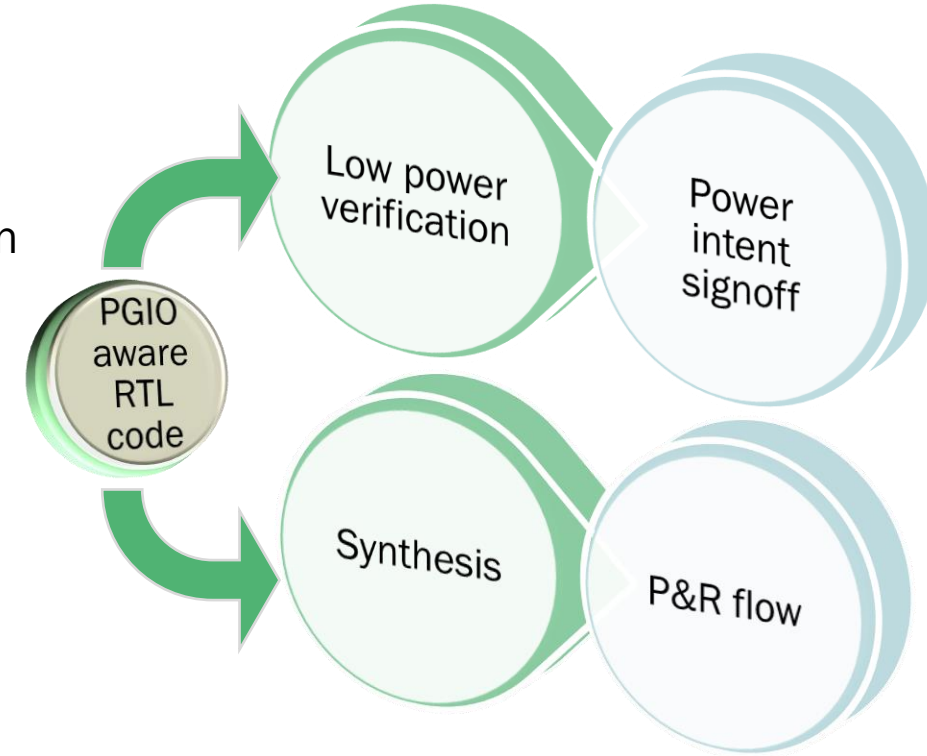
Timing

time_design Summary					Conventional
Setup mode	all	reg2reg	reg2cgate	default	
WNS (ns)	-2.059	-0.145	0.003	-2.059	
TNS (ns)	-11.550	-0.145	0.000	-11.406	
Violating Paths:	19	1	0	18	
All Paths:	58910	56648	2203	274	

					PGIO aware
Setup mode	all	reg2reg	reg2cgate	default	
WNS (ns)	-2.207	-0.142	0.005	-2.207	
TNS (ns)	-12.299	-0.142	0.000	-12.157	
Violating Paths:	19	1	0	18	
All Paths:	58919	56657	2203	274	

# Summary & Conclusion

- Early generation of PGIO aware RTL → **Concurrent execution of LP verification and PD**
- Fully automated power connection inferred LP mixed-signal implementation and verification → **Complete verification** at early stage (RTL)
- Compatible with standard/semi-custom implementation and coherence across all flows
- Enabled verification of ESD protection integration aspects at early stage
- **What is verified is what is designed, built and what the end user sees!**
  - No custom forces for verification → Eliminate manual review(s)
- **Overall design cycle time and RTL freeze quality improved**



# References

1. Lakshmanan B et al., “Extended Power Connectivity Solution for CPF based Low Power Simulation,” DAC 2021
2. Sooraj Sekhar et al., “Optimal and Efficient Power Aware Verification Framework for Low Power Mixed-Signal SoC,” DAC 2022
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[https://support.cadence.com/apex/RedirectPage?urlType=techPubs&url=/tech-pubs/Docs/genus\\_user/genus\\_user21.1/genus\\_user.pdf](https://support.cadence.com/apex/RedirectPage?urlType=techPubs&url=/tech-pubs/Docs/genus_user/genus_user21.1/genus_user.pdf)
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# Thank you



**TEXAS INSTRUMENTS**

